UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	35.C13388
First Named Inventor or Application Identifier	
MAHITO SHINOHARA	
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [ ] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification — *Total Pages* 19
3. [X] Drawings *(35 USC 113)* — *Total Sheets* 3
4. [X] Oath or Declaration — *Total Pages* 1
   - a. [ ] Newly executed (original or copy)
   - b. [X] Unexecuted for information purposes
   - c. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
     - i. [ ] DELETION OF INVENTOR(S) Signed Statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4c is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4c, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: _____

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. _/____

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label — 05514 (Insert Customer No. or Attach bar code label here) — or [ ] Correspondence address below

NAME					
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City		State		Zip Code	
Country		Telephone		Fax	

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	16-20 =	0	X $ 18.00 =	$ -0-
	INDEPENDENT CLAIMS (37 cfr 1.16(b))	3-3 =	0	X $ 78.00 =	$ -0-
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			$260.00 =	$ -0-
				BASIC FEE (37 CFR 1.16(a))	$ 760.00
			Total of above Calculations =		$ 760.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				
				TOTAL =	$ 760.00

19. Small entity status

a. ☐ A Small entity statement is enclosed

b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.

c. ☐ Is no longer claimed.

20. ☒ A check in the amount of $ 760.00 to cover the filing fee is enclosed.

21. ☐ A check in the amount of $ _____ to cover the recordal fee is enclosed.

22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

a. ☒ Fees required under 37 CFR 1.16.

b. ☐ Fees required under 37 CFR 1.17.

c. ☐ Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	Abigail F. Cousins (29,292)
SIGNATURE	Abigail Cousins
DATE	March 9, 1999

F509\A637254\jrl

SOLID STATE IMAGE PICKUP DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to driving control for a solid state image pickup device.

Related Background Art

Conventionally there is known a method for driving a solid state image pickup device as shown in Fig. 1, in which there are shown an image sensor chip 1, a drive timing control device 2 such as a microcomputer (hereinafter called microcomputer) for controlling the image sensor chip 1 by outputting driving pulses therefore, drive mode control wirings 3, drive pulse wirings 5, a reference clock wiring 6, a drive pulse generation circuit 21 provided in the image sensor chip 1, and an image pickup unit/peripheral circuit 22 including plural photoelectric converting elements etc. and a peripheral circuit including horizontal and vertical scanning circuits.

Fig. 2 shows another conventional configuration, wherein shown are an image sensor chip 1 including the image pickup unit/peripheral circuit 22 shown in Fig. 3 a drive pulse generation circuit 4, drive pulse wirings 5. The drive pulse generation circuit 4 is not integrated in an image sensor chip. In Fig. 2, the microcomputer 2, the drive mode control wirings 3 and

the reference clock wiring 6 are same as those in Fig. 1.

In the configuration shown in Fig. 1, the image sensor for outputting the image signal is operated by driving the image pickup unit and peripheral circuit 22 either directly by the drive mode control wirings 3 and the reference clock wiring 6 or by drive pulses generated in a circuit in the image sensor chip based on the drive mode control wirings 3 and the reference clock wiring 6. The configuration shown in Fig. 2 is employed in case requiring drive pulses of a strong driving force, wherein the required drive pulses are generated by the chip of the drive pulse generation circuit 4, based on the drive mode control wirings 3 and the reference clock wiring 6.

In either case, the operation mode of the image sensor chip 1 and the timing thereof are determined by the drive timing controlling device 2 such as the microcomputer, and the microcomputer 2 has to be operated in order to drive the image sensor chip 1.

However such conventional operation of the image sensor chip solely by the external drive causes a drawback in certain situations.

For example, such drawback occurs in a case where the image sensor chip performs a preliminary operation and a main operation, in which the main operation accesses the required image information, and the

preliminary operation monitors the projection of the required image onto the image sensor chip. In such process, the main operation starts after the necessary image is projected on the image sensor chip in the preliminary operation, but the preliminary operation may continue for a long period during which the microcomputer 2 and the drive pulse generation circuit 4 have to be continuously operated, so that the consumption of the electric power continues even while the access of the required image information does not take place.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a solid state image pickup device, capable of saving the electric power consumption.

The above-mentioned object can be attained, according to an aspect of the present invention, by a solid state image pickup device in which a reference clock generation circuit for determining the basic timing of the drive pulses for the image pickup unit is formed in a same semiconductor chip as that of the image pickup unit or the drive pulse generation circuit.

According to an another aspect of the present invention, there is provided a solid state image pickup device comprising an image pickup unit including plural

photoelectric conversion elements, a drive pulse generation circuit for driving the image pickup unit, a reference pulse generation circuit for determining the timing of the drive pulses, a first control circuit for controlling the operation mode of the drive pulse generation circuit, a second control circuit for controlling the operation mode of the drive pulse generation circuit, and a switch for connecting either the first control circuit or the second control circuit to the drive pulse generation circuit.

Other objects of the present invention, and the features thereof, will become fully apparent from the following description, which is to be taken in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 are views showing conventional configurations;

Fig. 3 is a block diagram showing a first embodiment of the present invention; and

Fig. 4 is a block diagram showing a second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following there will be given a detailed explanation on the first embodiment of the present invention, with reference to the attached drawings.

Fig. 3 shows a solid state image pickup device constituting the first embodiment, wherein shown a sensor chip 1 constituted, for example, by a sensor unit 30 including an image pickup unit containing photoelectric conversion elements and peripheral circuits containing horizontal and vertical scanning circuits for reading the charges converted from light by the photoelectric conversion elements, and a drive pulse generation circuit 21; a drive timing control device 2 such as a microcomputer (hereinafter called microcomputer) for controlling the sensor chip 1 by outputting the drive pulses of the main operation mode thereof; drive mode control wirings 3 for the main operation mode from the microcomputer 2; a reference clock wiring 6 for the main operation mode; and drive pulse wirings 5.

There are also shown a reference clock generation circuit 7 for the preliminary operation mode; a preliminary operation mode generation circuit 8 for generating a preliminary operation mode clock signal based on the reference clock signal generated by the reference clock generation circuit 7; a switch 9 for selecting either the clock signal from the microcomputer 2 or the clock signal of the reference clock generation circuit 7 and the preliminary operation mode generation circuit 8; and an output line 10 from the microcomputer 2 for selecting the state of

the switch 9. The voltage on the output line 10 is for example at a low level in case the microcomputer 2 is turned off, whereby the switch 9 selects the outputs of the internal reference clock generation circuit 7 and the preliminary operation mode generation circuit 8, but assumes a high level in case the microcomputer 2 is turned on whereby the switch 9 selects the pulses of the drive mode control wirings 3 and the reference clock wiring 6 from the microcomputer 2 .

There are further provided a detection circuit 11 for detecting whether the output of the sensor unit in the preliminary operation mode contains a necessary image signal, and a latch circuit 12 for latching the output of the detection circuit 11, and the output 13 of the latch circuit 12 is transmitted to the microcomputer 2. A switch 14 transmits the output of the sensor either to the image detection circuit 11 or the microcomputer. For example the voltage of the output 13 can be selected as high or low respectively when the image pickup unit fetches or not the necessary image. In such situation, the microcomputer 2 in the off state can be turned on by a shift of the output 13 from the low level to the high level, whereby the operation of the image sensor can shift from the preliminary operation under the control of the reference clock generation circuit 7 and the preliminary operation mode generation circuit 8 to the

main operation under the control of the microcomputer 2.

The microcomputer 2 can access the necessary image information exactly from the sensor output 20 in the main operation. A drive pulse generation circuit 21 gives various drive pulses such as drive pulses for horizontal scanning, drive pulses for vertical scanning, and a reset pulse for the image pickup unit etc., to the sensor unit.

In the following there will be explained the operation of the present embodiment.

At first, in the preliminary operation mode, the clock pulses from the preliminary operation mode generation circuit and from the reference clock generation circuit are input, respectively through the switches 9-1, 9-2 into the drive pulse generation circuit. Also the switch 14 switches the sensor output into the detection circuit 11.

Based on the signals from the reference clock generation circuit and the preliminary operation mode generation circuit, the drive pulse generation circuit transmits pulses to the horizontal and vertical scanning circuits, thereby reading the signals from the photoelectric conversion elements of the sensor unit. The signals read from the sensor unit are entered into the image detection circuit, and, if the necessary image is detected, the output of the latch circuit is

shifted to a high level state whereby the microcomputer is turned on. At the same time the switch 9 is so shifted that the signal from the microcomputer is supplied to the drive pulse generation circuit. Also the switch 14 is so shifted that the sensor output is connected to the microcomputer.

Based on the control signal from the microcomputer, the drive pulse generation circuit sends pulses to the horizontal and vertical scanning circuits, whereby the signals are read from the photoelectric conversion elements of the sensor unit. The signals read from the sensor unit are entered into the microcomputer and subjected to image signal processing such as color processing, white balancing etc. to obtain an image signal.

The above-described embodiment allows to reduce the wasteful power consumption in the microprocessor, by turning off the microcomputer 2 in the preliminary operation because only a simple signal process is executed, and starting the control by the microcomputer in the main operation in which the image information has to be fetched. The preliminary operation reduces power consumption by operating low-resolution readout, and by performing an intermittent operation, for example every 500 ms. Such intermittent operation can be realized by counting the reference clock signals with a counter.

Specifically, in the preliminary operation, the preliminary operation mode generation circuit 8 generates a drive control signal of the preliminary operation mode based on the reference clock signal generated by the reference clock generation circuit 7 on the image sensor chip, and the drive pulse generation circuit 21 generates drive pulses based on the generated drive control signal to drive the peripheral scanning circuits. The image pickup unit sequentially reads out the image signal corresponding to light received in the preliminary operation mode. In the case that the image detection circuit 11 determines that the sensor receives the necessary image, the latch circuit 12 is latched. This determination may be attained by simple image detection, such as detection of an image signal component whose level is greater than a predetermined level. In the preliminary operation, it is therefore possible in a scanning and read-out operation to reduce the number of the horizontal and vertical scanning lines in image signal reading to a half of that in the main operation mode or to perform the operation intermittently, since the sensor is operated as a monitor to merely determine whether or not the sensor receives the necessary image. The power consumption in this case can be significantly reduced not only in the microcomputer but also in the solid state image pickup

device.

In the following there will be given a detailed explanation on the second embodiment of the present invention, with reference to the attached drawings.

Fig. 4 shows the second embodiment of the present invention. An image sensor chip 1 is driven by a drive pulse generation chip 4. In Fig. 4, the image sensor chip 1, microcomputer 2, drive mode control pulse 3, drive pulse generation chip 4, drive pulse 5, reference clock pulse 6, reference clock generation circuit 7, operation mode generation circuit 8, switch 9, mode switching selection pulse 10, image detection circuit 11, latch 12, image detection discriminating output 13, drive pulse generation circuit 21, and sensor output 20 in the microcomputer control are same as those shown in Fig. 3 and will not be explained again.

In this configuration, though the entire device is composed of the image sensor chip 1 and the drive pulse generation chip 4, the latter is provided therein with the reference clock generation circuit 7, the operation mode generation circuit 8 and the switch 9, so that, in the preliminary operation, the image pickup unit and the peripheral scanning circuit 2 in the image sensor chip 1 are operated in synchronization with the reference clock signal generated in the reference clock generation circuit 7, thereby outputting the image signal to the sensor output 14.

Also in the main operation, the reference clock pulse 6 and the drive mode control pulse 3 are supplied to the drive pulse generation circuit 21 according to the reference clock signal in the microcomputer 2 to operate the image pickup unit and the peripheral scanning circuit 22 in the image sensor chip 1, thereby outputting the image signal to the sensor output 14.

In the second embodiment shown in Fig. 4, in the preliminary operation, the image sensor chip 1 operates at the timing of the reference clock generation circuit 7 formed in the drive pulse generation chip 4, and the microcomputer 2 remains in the turned-off state.

As in the first embodiment, the control is switched to the microcomputer 2 when it is turned on, thereby suppressing the power consumption of the microcomputer 2 in the preliminary operation and also suppressing the power consumption in the entire device.

As explained in the foregoing, the first and second embodiments allow to select the drive mode control for the sensor unit by the external microcomputer or by the reference clock generation circuit and the operation mode generation circuit formed on the image sensor chip or on the drive pulse generation circuit chip, whereby it is rendered possible to suspend the operation of the microcomputer during the preliminary operation mode in which the signal processing by the external microcomputer is not

required, thereby suppressing the wasteful power consumption in the microcomputer.

Also in the preliminary operation, further suppression of the power consumption is possible since the image pickup unit and the peripheral scanning circuit can be independently operated on the image sensor chip or the drive pulse generation circuit chip.

In the foregoing first and second embodiments, the sensor unit, the reference clock generation circuit, the drive pulse generation circuit etc. are assumed to be integrated into a single chip, but it is also possible to integrate the sensor unit and the reference clock generation circuit only in a chip. It is thus possible to change the combination of the circuits to be integrated in a single chip, or to form such circuits as separate components.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

WHAT IS CLAIMED IS:

1. A solid state image pickup device comprising:

an image pickup unit including plural photoelectric conversion elements; and

a reference clock generation circuit for determining the timing of a drive pulse;

wherein said image pickup unit and said reference clock generation circuit are formed in a same semiconductor chip.

2. A solid state image pickup device according to claim 1, further comprising:

a drive pulse generation circuit for driving said image pickup unit;

wherein said drive pulse generation circuit is formed in said semiconductor chip.

3. A solid state image pickup device according to claim 1, wherein a preliminary control circuit for driving said image pickup unit in a predetermined preliminary operation mode is formed on said semiconductor chip.

4. A solid state image pickup device according to claim 2, wherein a preliminary control circuit for driving said image pickup unit in a predetermined preliminary operation mode is formed on said

semiconductor chip.

5. A solid state image pickup device according to claim 3, wherein a switch for supplying the drive pulse generation circuit of said semiconductor chip selectively with a reference clock signal from said reference clock generation circuit incorporated in said semiconductor chip and a drive mode control clock signal from said preliminary control circuit, or a reference clock signal and a drive mode control clock signal from the exterior of said semiconductor chip, is formed on said semiconductor chip.

6. A solid state image pickup device according to claim 4, wherein a switch for supplying the drive pulse generation circuit of said semiconductor chip selectively with a reference clock signal from said reference clock generation circuit incorporated in said semiconductor chip and a drive mode control clock signal from said preliminary control circuit, or a reference clock signal and a drive mode control clock signal from the exterior of said semiconductor chip, is formed on said semiconductor chip.

7. A solid state image pickup device according to claim 3, wherein said device has a preliminary operation mode for operating said image pickup unit in

synchronization with the reference clock signal and the preliminary operation control clock signal from said reference clock generation circuit and said preliminary operation control circuit integrated in said semiconductor chip, and a main operation mode for operating said image pickup unit in synchronization with the reference clock signal and the drive mode control clock signal from the exterior of said semiconductor chip, wherein the operation in said semiconductor chip is executed with a power consumption lower in said preliminary operation mode than in said main operation mode.

8. A solid state image pickup device according to claim 4, wherein said device has a preliminary operation mode for operating said image pickup unit in synchronization with the reference clock signal and the preliminary operation control clock signal from said reference clock generation circuit and said preliminary operation control circuit integrated in said semiconductor chip, and a main operation mode for operating said image pickup unit in synchronization with the reference clock signal and the drive mode control clock signal from the exterior of said semiconductor chip, wherein the operation in said semiconductor chip is executed with a power consumption lower in said preliminary operation mode than in said

main operation mode.

9. A solid state image pickup device provided with a solid state image pickup chip including an image pickup unit and a drive pulse generation circuit chip including a drive pulse generation circuit for driving said image pickup unit, wherein a reference clock generation circuit for determining the timing of the drive pulse is formed in said drive pulse generation circuit chip.

10. A solid state image pickup device according to claim 9, wherein a preliminary control circuit for driving said state image pickup chip in a predetermined drive mode is formed in said drive pulse generation circuit chip.

11. A solid state image pickup device according to claim 10, wherein a switch for supplying the drive pulse generation circuit of said semiconductor chip selectively with a reference clock signal from said basic clock generation circuit incorporated in said reference pulse generation circuit chip and a drive mode control clock signal from said preliminary control circuit, or a reference clock signal and a drive mode control clock signal from the exterior of said semiconductor chip, is formed on said drive pulse

generation circuit chip.

12. A solid state image pickup device according to claim 10, wherein said device has a preliminary operation mode for operating said image pickup unit in synchronization with the reference clock signal and the preliminary operation control clock signal from said reference clock generation circuit and said preliminary operation control circuit integrated in said drive pulse generation circuit chip, and a main operation mode for operating said image pickup unit in synchronization with the reference clock signal and the drive mode control clock signal from the exterior of said chip, wherein the operation in said chip is executed with a power consumption lower in said preliminary operation mode than in said main operation mode.

13. A solid state image pickup device comprising:

an image pickup unit including plural photoelectric conversion elements;

a drive pulse generation circuit for driving said image pickup unit;

a reference pulse generation circuit for determining the timing of a drive pulse;

a first control circuit for controlling the

operation mode of said drive pulse generation circuit;

a second control circuit for controlling the operation mode of said drive pulse generation circuit; and

a switch for connecting said first control circuit or said second control circuit to said drive pulse generation circuit.

14. A solid state image pickup device according to claim 13, wherein said switch is adapted to turn off the power supply to said first or second control circuit which is not connected to said drive pulse generation circuit.

15. A solid state image pickup device according to claim 13, wherein said first control circuit functions with a lower electric power consumption than in said second control circuit.

16. A solid state image pickup device according to claim 15, further comprising:

a signal processing unit for executing image processing on the signal from said image pickup unit;

wherein said signal processing unit is controlled by said second control circuit.

ABSTRACT OF THE DISCLOSURE

There is provided a solid state image pickup device provided with an image pickup unit containing plural photoelectric conversion elements and a reference clock generation circuit for determining the timing of the drive pulse, wherein the image pickup unit and the reference clock generation circuit are formed in a same semiconductor chip in order to reduce the electric power consumption.

FIG.1

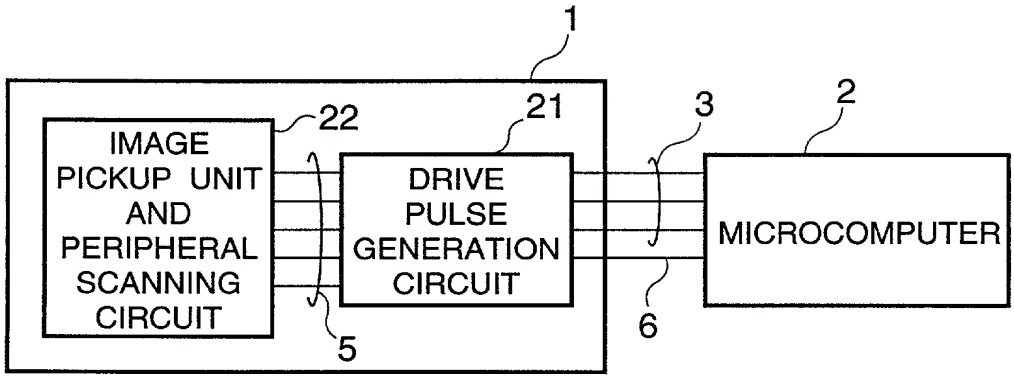

1
22
21
3
2
IMAGE PICKUP UNIT AND PERIPHERAL SCANNING CIRCUIT
DRIVE PULSE GENERATION CIRCUIT
MICROCOMPUTER
5
6

FIG.2

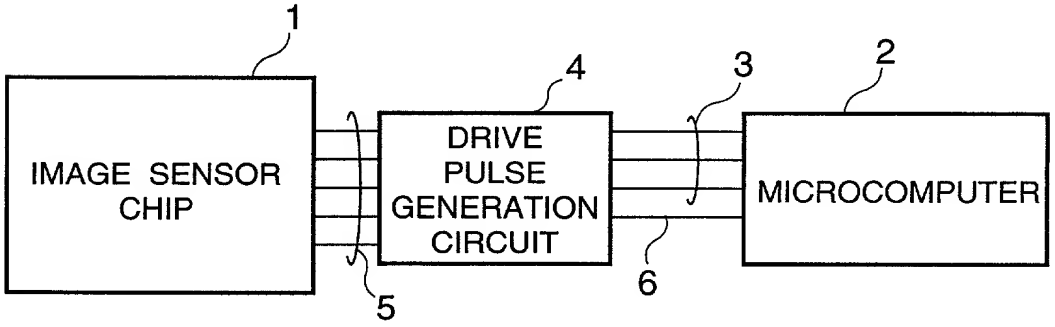

1
4
3
2
IMAGE SENSOR CHIP
DRIVE PULSE GENERATION CIRCUIT
MICROCOMPUTER
5
6

FIG.3

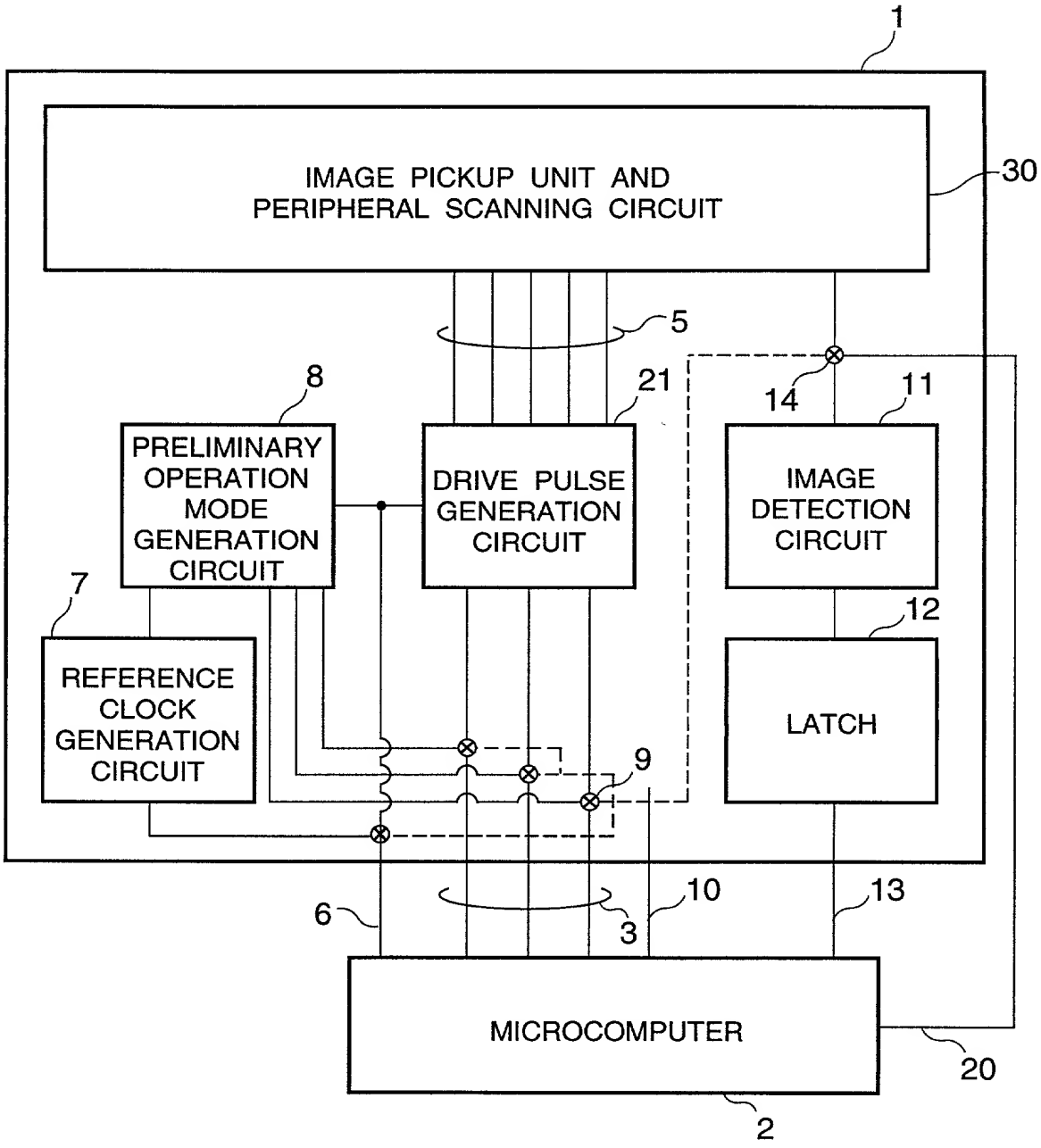
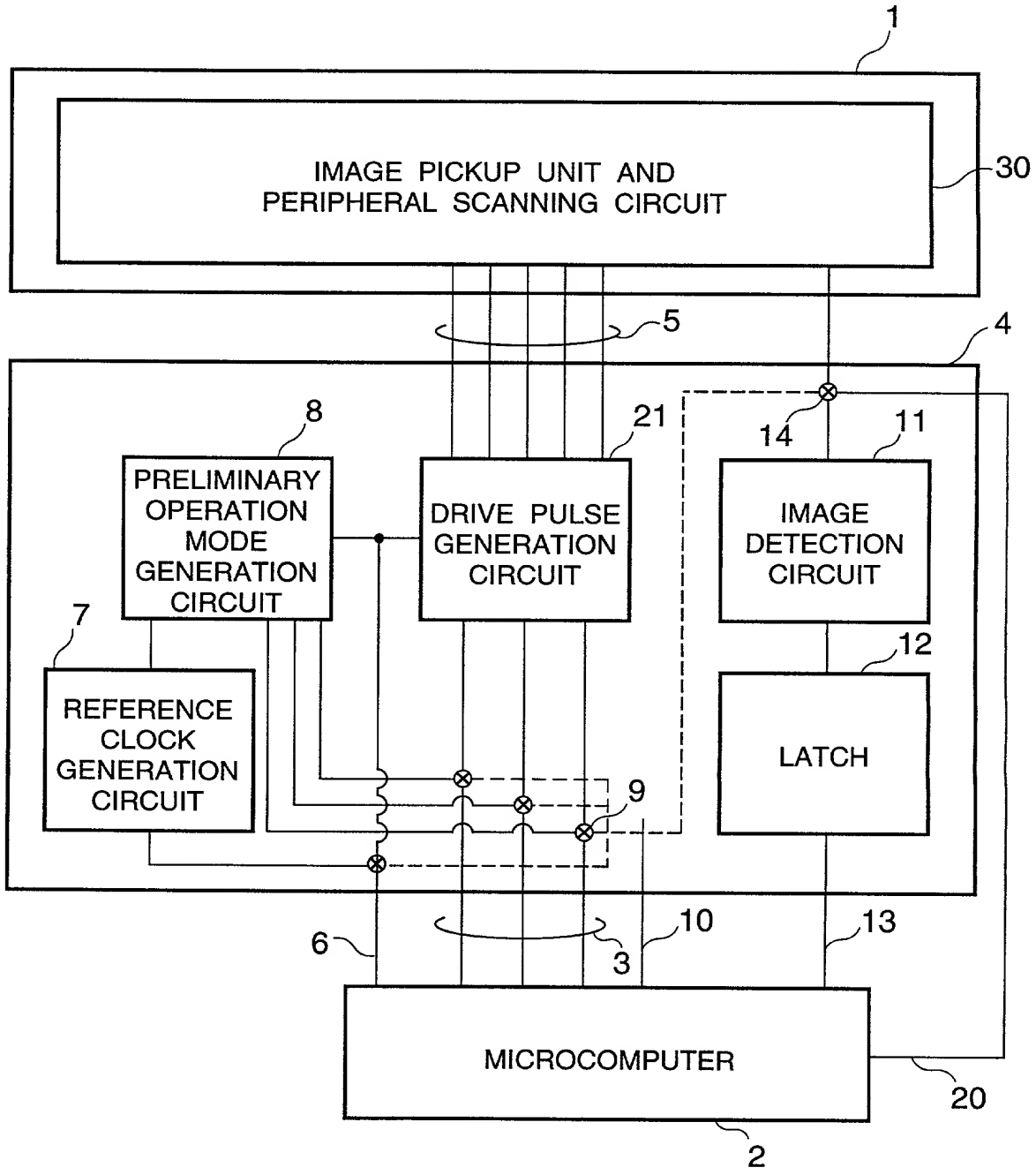

1
IMAGE PICKUP UNIT AND PERIPHERAL SCANNING CIRCUIT
30
5
8
21
14
11
PRELIMINARY OPERATION MODE GENERATION CIRCUIT
DRIVE PULSE GENERATION CIRCUIT
IMAGE DETECTION CIRCUIT
7
12
REFERENCE CLOCK GENERATION CIRCUIT
LATCH
9
6
3
10
13
MICROCOMPUTER
20
2

FIG.4


1
IMAGE PICKUP UNIT AND
PERIPHERAL SCANNING CIRCUIT
30
5
4
8
21
14
11
PRELIMINARY
OPERATION
MODE
GENERATION
CIRCUIT
DRIVE PULSE
GENERATION
CIRCUIT
IMAGE
DETECTION
CIRCUIT
7
12
REFERENCE
CLOCK
GENERATION
CIRCUIT
LATCH
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MICROCOMPUTER
20
2

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
(Page 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SOLID STATE IMAGE PICKUP DEVICE,

the specification of which [X] is attached hereto [ ] was filed on _____ as United States Application No. or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b), of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed
Japan	10-061230	March 12, 1998	Yes

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Application No.	Filed (Day/Mo./Yr.)	Status (Patented, Pending, Abandoned)

I hereby appoint the practitioners associated with the firm and Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole or First Inventor MAHITO SHINOHARA

Inventor's signature _____

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